E&ICT Academy, PDPM IIITDM Jabalpur

Online Winter Faculty Development Programme
VLSI Design using Open source tools

February 10 - 21, 2025 : Online live streaming

Jointly Organized by

IIT Guwahati   IIITDM Jabalpur   IIT Roorkee   NIT Patna   MNIT Jaipur

Schedule and Course Contents

[February 10 - 21, 2025, 02:00 PM to 06:00 PM]

- Introduction to VLSI design flow.
- Introduction to High Level Synthesis, Intel HLS Compiler and System Integration, HLS Implementation, Software design with the new HLS Component system
  Introduction to Intel SoC FPGAs, Basic SoC lab demo with hands on
- High level synthesis- scheduling, binding
- Logic synthesis- two level, multilevel logic optimization, encoding
- Sequential circuit optimization, FSM synthesis, retiming, state encoding
- Library binding
- Physical design- partiioning, placement, floor planning, global & channel routing
- Layer and Power Planning
- Delay Calculations and System Implications
- Setup and Hold Discussion Placement Basics and Settings
- DRC LVS and Extraction
- Low Power Flow Basics
- Sign Off

Coordinators

Dr Pushpa Raikwal,
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RESOURCE PERSONS

- Dr. Sarfraz Hussain, SoECE, REVA University, Bangalore
- Dr. Amol Boke, Nine Labs, IIT Guwahati
- Dr. Bikram Paul, SCEE, IIT Mandi
- Dr. Rahul Shrestha, IIT Mandi
- Dr. Shaik Rafi Ahamed, IIT Guwahati

Registration Details

Registration link – Please fill in the registration form using the following link:
https://forms.gle/uTxD6ZTr56QEMsXz8

Registration fee: INR 500/-
Last Date for Registration: February 03, 2025

Online payment details:
- Internet banking
  Beneficiary Name: PDPM IIITDM Jabalpur
  Bank Name: INDIAN BANK
  A/C No. : 50018692852
  IFSC Code: IDIB000M694

- UPI ID: iiitdmj@indianbk

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